DERWENT-ACC-NO: 2002-704238

DERWENT-WEEK: 200276

TITLE: Method for fabricating capacitor of semiconductor device

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PATENT-ASSIGNEE: HYNIX SEMICONDUCTOR INC[HYNIN]

PRIORITY-DATA: 2000KR-0067707 (November 15, 2000)

PATENT-FAMILY:

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KR 2002037804 A	May 23, 2002	N/A	001	H01L 027/108

APPLICATION-DATA:

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KR2002037804A	N/A	2000KR-0067707	November 15, 2000

INT-CL (IPC): H01L027/108

ABSTRACTED-PUB-NO: KR2002037804A

BASIC-ABSTRACT:

NOVELTY - A method for fabricating a capacitor of a semiconductor device is provided to prevent a **Pt seed** from being lifted by an attack of an interlayer dielectric under the seed Pt, by forming a barium, strontium and titanium (BST) capacitor.

DETAILED DESCRIPTION - An oxide material (1) and a silicon nitride material(2)
are formed on a substrate to insulate the substrate from the capacitor. After a contact hole for a vertical interconnection between the substrate and the

capacitor is formed, a doped polycrystalline silicon plug is formed. A plug recess is formed. Ti is deposited on the substrate to reduce contact resistance between the plug and a barrier metal(5). TiSix is formed through a heat treatment process, and the remaining Ti is eliminated. A barrier metal is deposited and planarized. A silicon nitride layer is deposited and etched back to cap the oxide material. A seed Pt layer(6) is deposited. A non-conductive material is deposited on the seed Pt layer and is patterned to form a dummy pattern. A surface treatment process is performed to eliminate contaminant on the surface of the seed Pt layer. An electroplating Pt layer(8) is deposited. The dummy pattern is removed. The seed Pt layer is removed. A chemical vapor
deposition (CVD) BST layer(9) is formed. The CVD BST layer is crystallized by a rapid thermal process(RTP) method. An upper electrode(10) is formed.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: METHOD FABRICATE CAPACITOR SEMICONDUCTOR DEVICE

DERWENT-CLASS: L03 U11 U13 U14

CPI-CODES: L03-G04A; L04-C10; L04-C14A;

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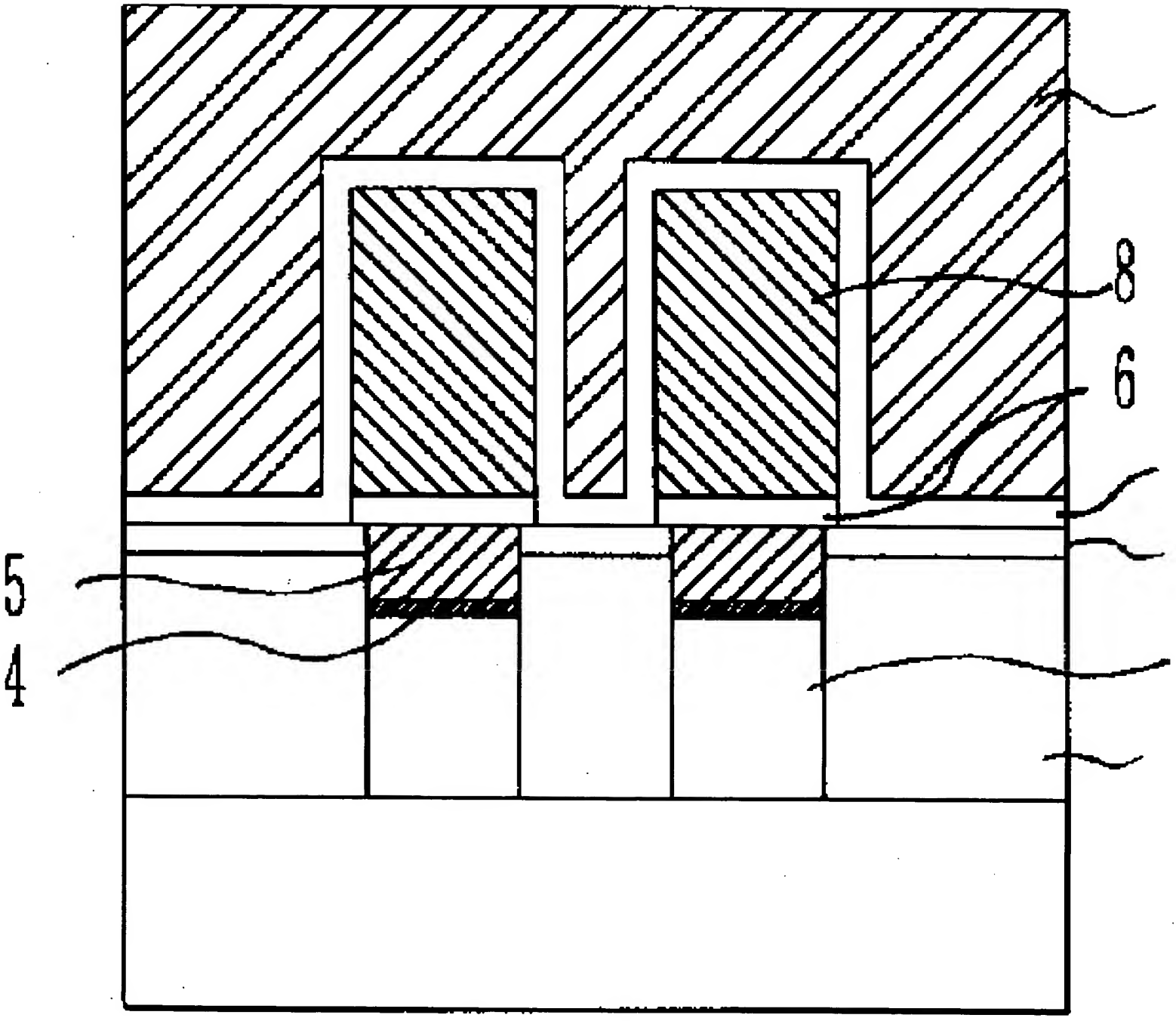
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